

Notice: This is not a final specification.
Outline, some parametric limits and figures are subject to be changed

CONTACT IMAGE SENSOR

FW2R108

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1. Description

This specification is applied to FW2R108 Contact Image Sensor module.

2. Scope

This FW2R108 is a CIS consists of a Rod Lens Array, double color LED light source and an array of linear MOS image sensor.

3. Outline

Item	Specification	Note
Scanning width	108 mm	
Sensor element density	200 DPI	CNT=GND
Effective number of sensor elements	850 elements (Full 864 elements)	8 th to 857 th
Scanning speed	Color(RGB):117×3 μsec/line (RGB) Black & White: 117 μsec/line	
Clock speed	8.0MHz	Note
Rod lens array	Single row	
Light source	Red λp = 630nm ± 15nm 60mA Green λp = 520nm ± 15nm 60mA Blue λp = 465nm ± 10nm 60mA	LED At least two LED vendors.
Power supply	+5.0V x 80 mA	
Data output	1 analog output	Synchronous
Block diagram	Figure 5	
Dimensions	Figure 1	

Note Clock Speed f must satisfy the following status:
 $f > (n + 72) / tint$
 f : Clock speed
 n : Full sensor elements number of every block.
 200DPI:864
 tint: Scanning speed

4. Image Data Output Characteristics (Ta = 25°C)

The shipment test in SHEC is done on the condition of this table.

In Color Mode

Item	Symbol	Specification			Note
		Red	Green	Blue	
DC supply voltage	VDD	+5.0V			Detector, Logic
LED supply voltage	VLED	<3.0V	<5.0V	<5.0V	
LED supply current	ILED	60mA	60mA	60mA	
White image target		0.05 ~ 0.09 OD			
Timing diagram		Figure 6			
Dark Reference	Dref	(1,200mV)			4.1
Dark output minimum	Vdmin	-100 ~ +200mV			4.2
White output maximum	Vpmax	930 ±100 mV			4.3
Dark output uniformity	Ud	Less than Vpmax/3.1			4.4
White output uniformity	Uep	Less than 50%			4.5
MTF		20 % MIN	30 % MIN	15 % MIN	4.6 71.37 lppi
Linearity	Gamma	1.05 ± 0.05			
Linearity Uniformity	LU	Less than 6 %			4.7

In Black and White Mode

Item	Symbol	Specification			Note
		Red	Green	Blue	
DC supply voltage	VDD	+5.0V			Detector, Logic
LED supply voltage	VLED	<3.0V	0V	0V	
LED supply current	ILED	60mA	0mA	0mA	
White image target		0.05 ~ 0.09 OD			
Timing diagram		Figure 6			
Dark Reference	Dref	(1,200mV)			4.1
Dark output minimum	Vdmin	-100 ~ +200mV			4.2
White output maximum	Vpmax	930 ±100 mV			4.3
Dark output uniformity	Ud	Less than Vpmax/1.3			4.4
White output uniformity	UEp	Less than 50%			4.5
MTF		20 % MIN			4.6 71.37 lppi
Linearity	Gamma	1.05 ± 0.05			
Linearity Uniformity	LU	Less than 6 %			4.7

The output level of image signal like white and dark and MTF is defined at the point of “ts2” which described in section 6. A test target is set on the reading position described Figure 1.

4.1 Dref

Dark reference output. As shown in Figure 4, Dref appears from clock #55 to #62. Vdmin output value is based on Dref.

4.2 Vdmin

As shown in Figure 2, Vdmin is the minimum in the dark output signal (turning off the LED). The other parameters are defined by Vdmin as a reference.

4.3 Vpmax

As shown in Figure 2, Vpmax is the maximum white output signal and is defined by:

$$Vpmax = \text{MAX}[Vp(n)]$$

Vp(n) is the output signal of the n-th pixel using a white image target.

4.4 Ud

As shown in Figure 2, Ud is the output signal in the dark (turning off the LED) and is defined by;

$$Ud = Vdmax - Vdmin$$

Vdmax is the maximum output signal of the nth pixel in the dark

Vdmin is the minimum output signal of the nth pixel in the dark

4.5 UEp

UEp is the white output non-uniformity with dark signal subtracted and is defined by:

$$UEp = ((VEpmax - VEpmi) / (VEpmax)) \times 100\%$$

VEpmax = MAX[VEp(n)]; is the maximum effective output signal

VEpmi = MIN[VEp(n)]; is the minimum effective output signal

VEp(n) is the effective output signal of every pixel and is defined by:

$$VEp(n) = Vp(n) - Vd(n)$$

4.6 MTF

MTF is defined by:

$$MTF = \text{MIN}\{ [(Vmax - Vmin) / VEp] \} \times 100\%$$

Vmax is the maximum output signal using the MTF image target

Vmin is the minimum output signal using the MTF image target

VEp is the effective output signal .

4.7 LU

LUG is measured following procedure and defined;

Step1. Test Target

The white image target is used as a test target. This target must not be moved while this test is being operated.

Step2. LED adjustment

Tred, Tgrn, Tblu should be adjusted according to Figure 8 procedure.

Step3. Dark and White correction

Dark and White correction must be done for every each pixel.

Step4. LED on time set

Tred, Tgrn and Tblu should be changed as following;

$$Tred/2, Tgrn/2, Tblu/2$$

Step5. Compute LUG

LUG should be computed for each color as;

$$LUG = \sqrt{Dgave - Dgextm}$$

Dgave is the average of Vg(n). Vg(n) should be got more than 8 times sampling.

Step6. LED on time set

Tred, Tgrn and Tblu should be changed as followed and compute LUG regarding to Step5;

$$Tred/4, Tgrn/4, Tblu/4$$

Step7. LED on time set

Tred, Tgrn and Tblu should be changed as followed and compute LUG regarding to Step5;

$$Tred/8, Tgrn/8, Tblu/8$$

4.8 Correction of Dark and White uniformity

For the best performance two points correction (dark and white) is strongly recommended.

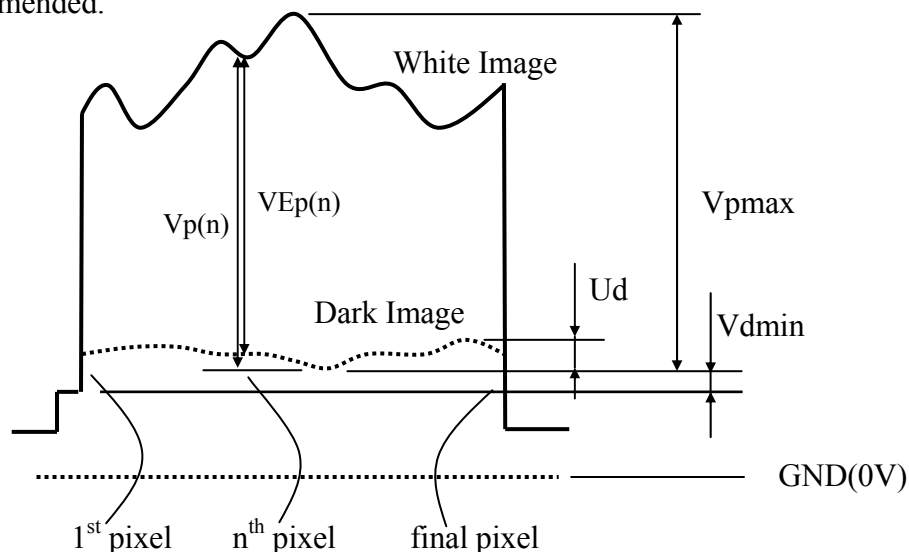


Figure 2. Output Signals Waveform

Dref

5. Maximum Rating

Item	Symbol	Specification	Note
DC supply voltage	VDD	+5.0V ± 0.25V	
Input voltage	VIN	0 ~ VDD+0.3V	SI, CLK
Ambient temperature	Ta	0 ~ +50 °C	Operating
		-20 ~ +60 °C	Non-operating
Ambient humidity		10 ~ 90%RH	Avoid a build up condensation
Maximum operating Temperature		65 °C 30minuts MAX	

LED

Parameter	Symbol	Red	Green	Blue	Notes
DC Forward Current	IF	60 mA	60 mA	60 mA	
Pulse Forward Current	IFP	60 mA	60 mA	60 mA	
DC Reverse Voltage	VR	5.0 V	5.0V	5.0V	

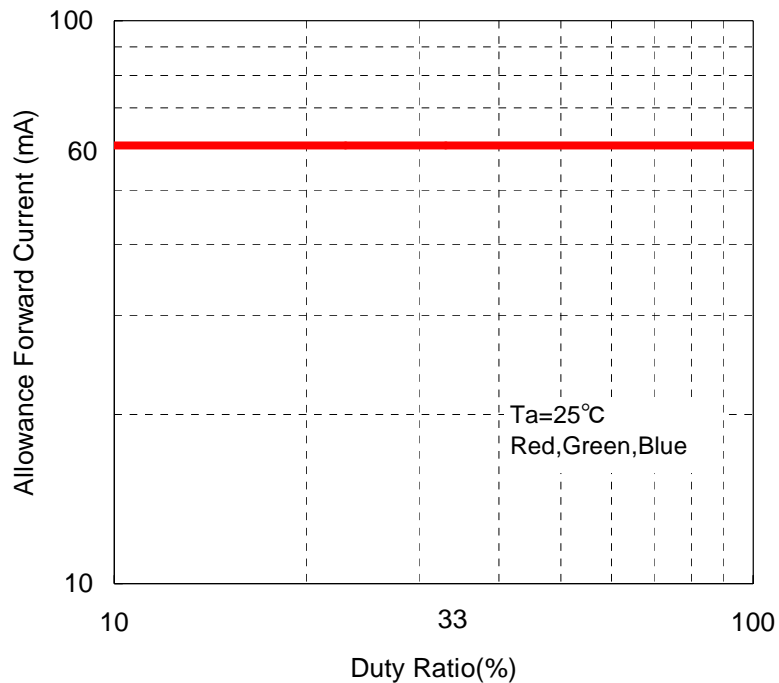
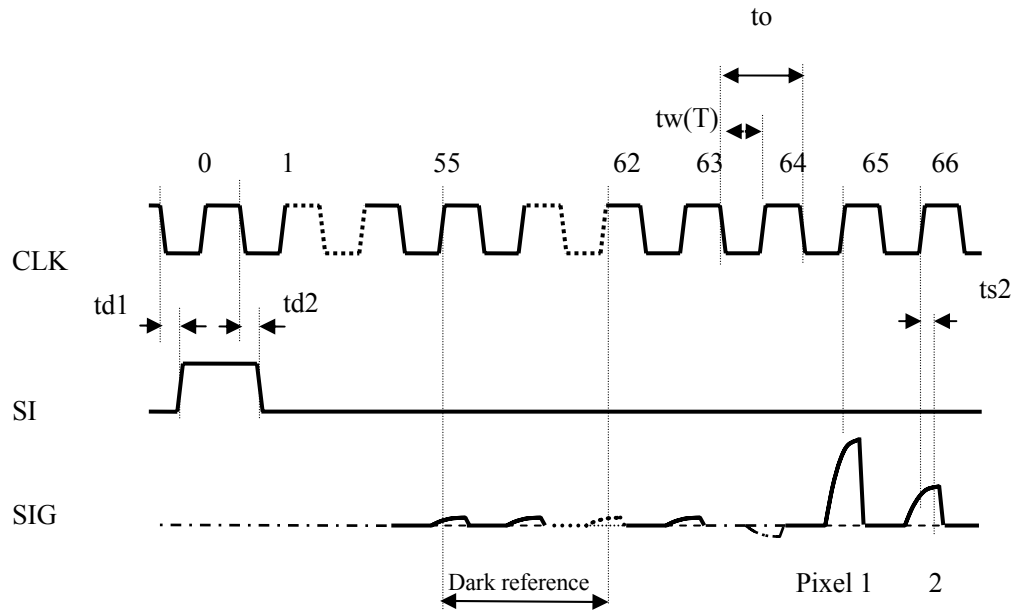


Figure 3. Duty Ratio vs Allowance Forward Current

6. Electrical Characteristics (Ta = 25 °C)

Item	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
DC Supply Voltage	VDD	GND reference	4.75	5.0	5.25	V
DC Supply Current	IDD	VDD = 5.0V		40	80	mA
LED Forward Voltage	VFred	IF=30mA	2.1	2.3	2.5	V
		IF=40mA	2.1	2.4	2.6	V
		IF=60mA	2.3	2.5	2.7	V
	VFgreen	IF=30mA	3.3	3.6	4.0	V
		IF=40mA	3.4	3.8	4.1	V
		IF=60mA	3.6	4.0	4.4	V
	VFblue	IF=30mA	3.3	3.7	4.1	V
		IF=40mA	3.4	3.8	4.2	V
		IF=60mA	3.6	4.0	4.3	V
Input voltage (Note 1)	VIH	SI, CLK	2.4			V
	VIL				0.8	V
Input Current Note 1	IIH	SI, CLK			5	mA
	IIL		-0.5			μA
Clock frequency	f	CLK	7.5	8.0	8.5	MHz
Clock pulse duty		tw(T)/to; to=1/f	48	50	52	%
SI delay time	td1	SI-CLK	10	30	to/2	ns
	td2	SI-CLK	10	30	to/2	ns
Data output stability time	ts2	CLK-SIG	5	10	15	ns

Note 1) 74HC244 or equivalent is recommended for input signal.



Dark reference for Dref appears between clock#55 to #62. Dark dummy stable time is as same as $ts2$.

Figure 4. Timing Diagram

7. Reliability

The following table satisfies the reliability when the CIS is operated continuously under standard operating conditions as specified in section 4.

Item	Variable Amount (%)	Note
White output	Initial level +10% -20%	1000Hr
	Initial level +10% -30%	5000Hr

8. Precautions before use:

8.1 Glass surface

The glass surface should be kept clean. Don't wipe the glass surface with hand. Don't use the CIS module in a dust-polluted environment. If the glass surface gets dirty, wipe the glass surface gently with a clean cloth soaked in alcohol. The glass surface should be wiped very carefully.

8.2 Extracting / Inserting the connector

The maximum number of times that the connector should be extracted and connected is 10. If the connector is inserted / extracted more than 10 times, the connector 'burrs' will be eroded, thereby making the connector ineffective.

8.3 Stable operation

(1) The connector pins should not be touched by bare hand or electrostatic charge materials.

(2) Noise

- a. Insert a low frequency noise suppressing capacitor (100uF) between VDD(+5.0V) and GND. A high frequency noise suppressing capacitor is already integrated into the circuit.
- b. Ensure that the sensor connecting cables are 30cm or less in length. The CLK and GND, SIG and GND and VLED and LEDr, LEDg, LEDb, respectively should form twisted cable pairs.

(3) Latch up

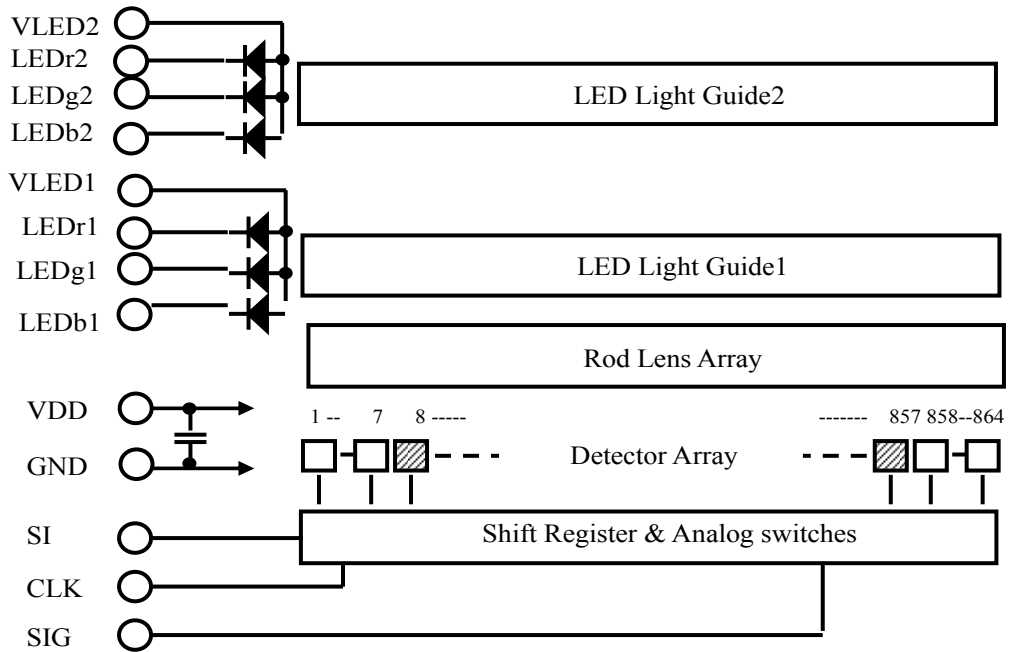
When the supply voltage is higher than the absolute maximum, latch up will cause the sensor to break, even if the voltage is caused by a surge. If the current varies rapidly in the external circuit, or when the power is turned on an off very frequently, ensure that the voltage of each terminal does not exceed the values indicated in below.

(4) LED circuit

As shown in Figure.6 LED circuit has not any resistance. Be careful not to connect the LED circuit to power supply directly without current limit resistors.

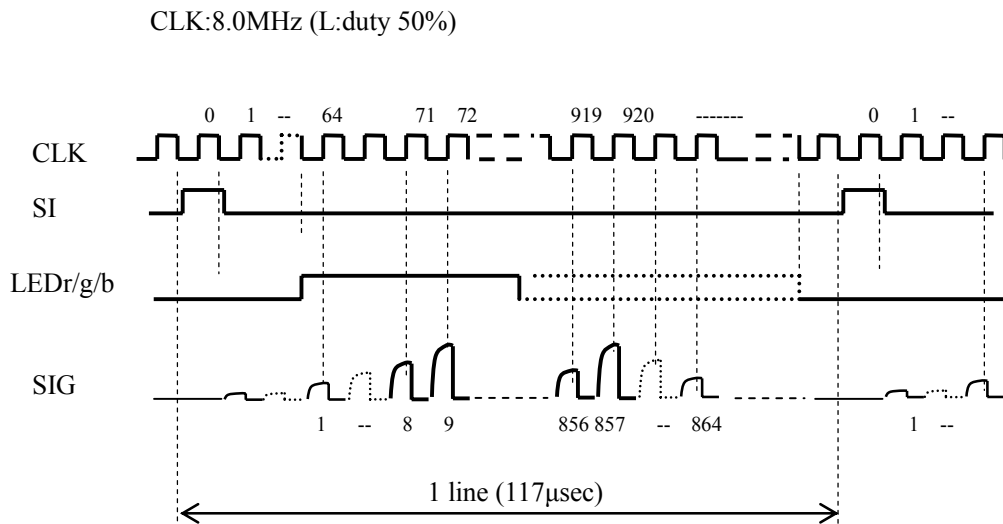
(5) Absolute maximum ratings

Item	Symbol	Condition	Specification		Unit
			Min	Max	
Supply Voltage	VDD	GND reference	-0.3	+6.5	V
Input voltage	Vin	SI,CLK	GND-0.3	VDD+0.3	V



Note: The outputs from 8th to 857th elements are effective image signal.

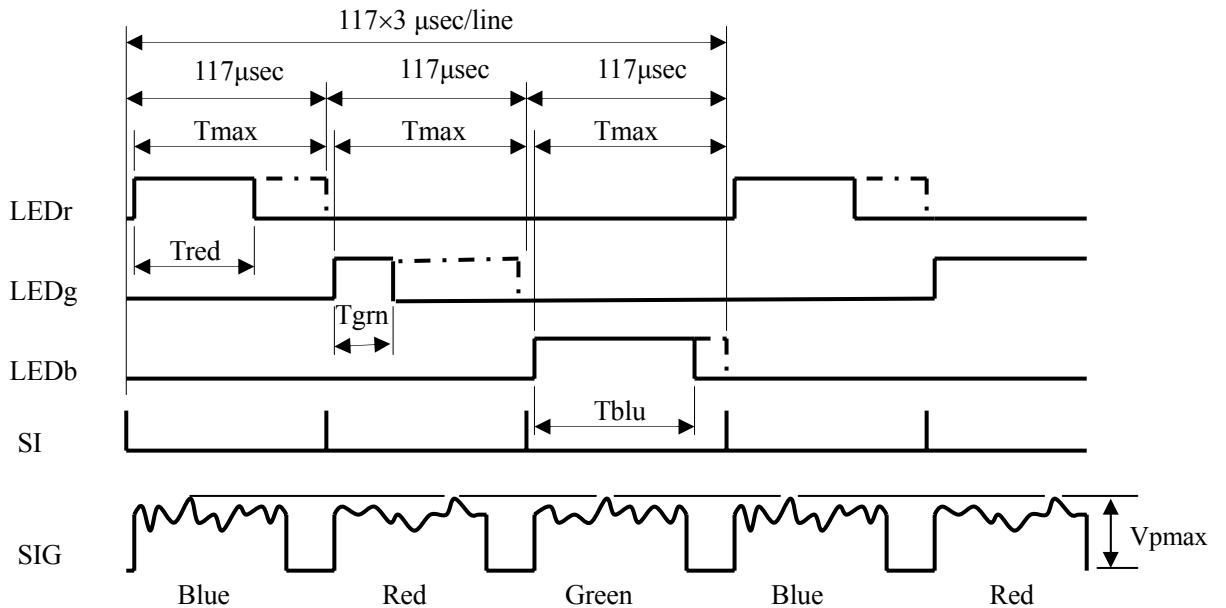
Figure 5. Block Diagram



Note: More than 7 clocks are needed after #864 video SIG.

Figure 6. Timing Diagram
(This is the SHEC shipping test condition)

□ **Color Mode**



V_{pmax} and the mean of $V_{\text{Ep}}(n)$ of all color have to be adjusted to nearly equal. Refer the adjustment flow at Figure 8.

**Figure 7. Color mode Timing Diagram
(This is the SHEC shipping test condition)**

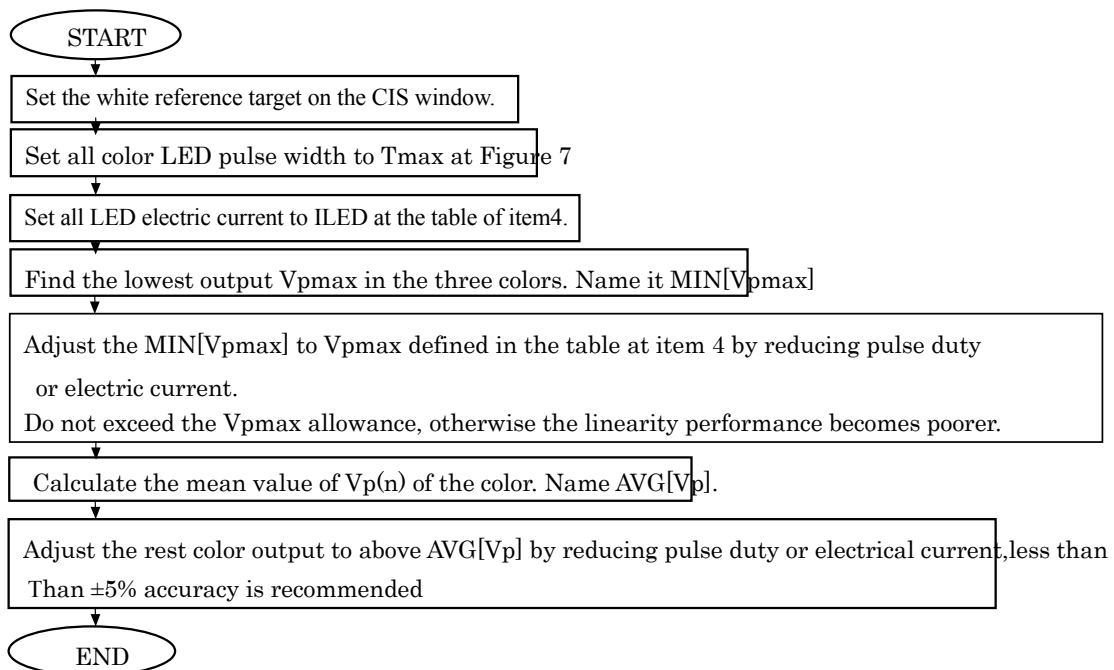
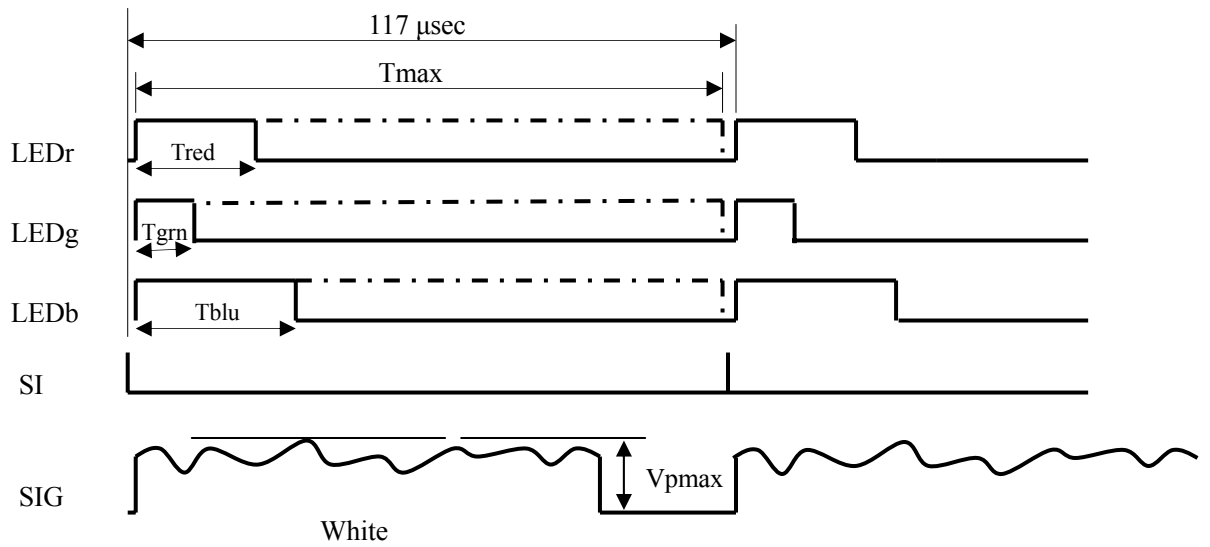


Figure 8. Flow Chart of Color mode Adjustment (This is the SHEC shipping test condition)

□ **B&W Mode White Light Source**



This is the sample of White light source application. Refer the adjustment flow chart at Figure 10.

Figure 9. B&W mode with White Light Source Timing Diagram

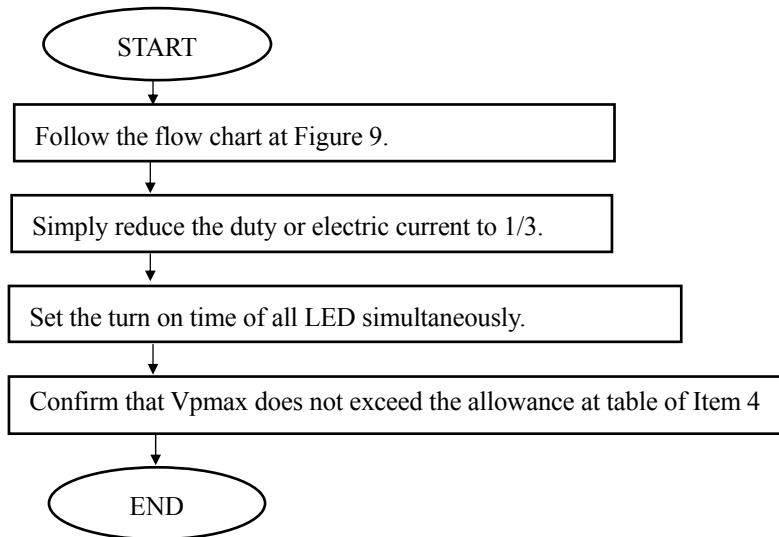
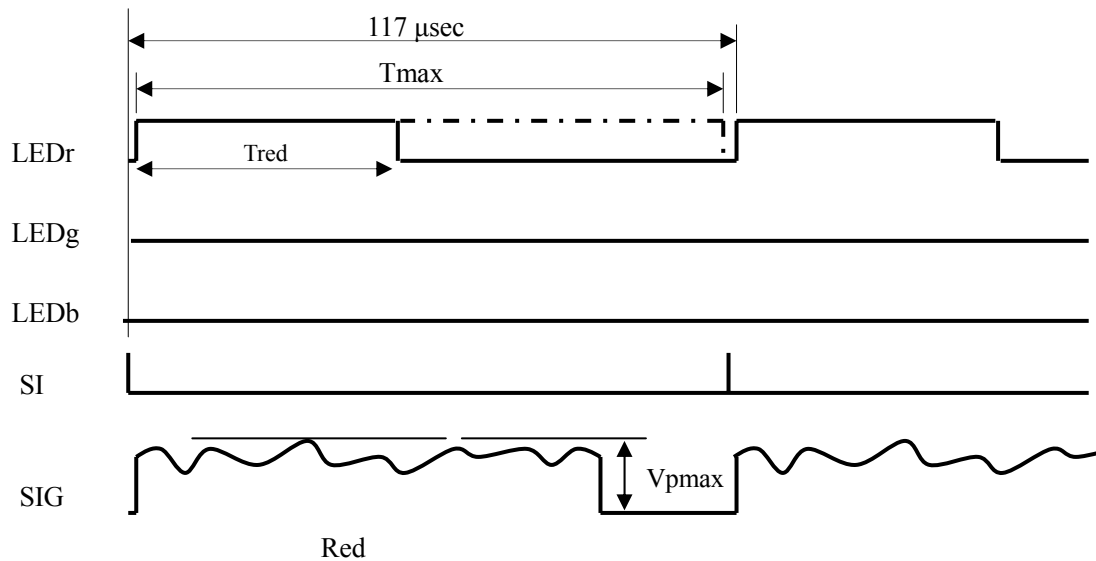


Figure 10. Flow Chart of B&W mode with White Light Source Adjustment

□ **B&W Mode with Mono-Color Light Source**



This is the example for Red Mono-Color application. Refer the adjustment flow chart at Figure 12.

Figure 11. B&W mode with White Light Source Timing Diagram

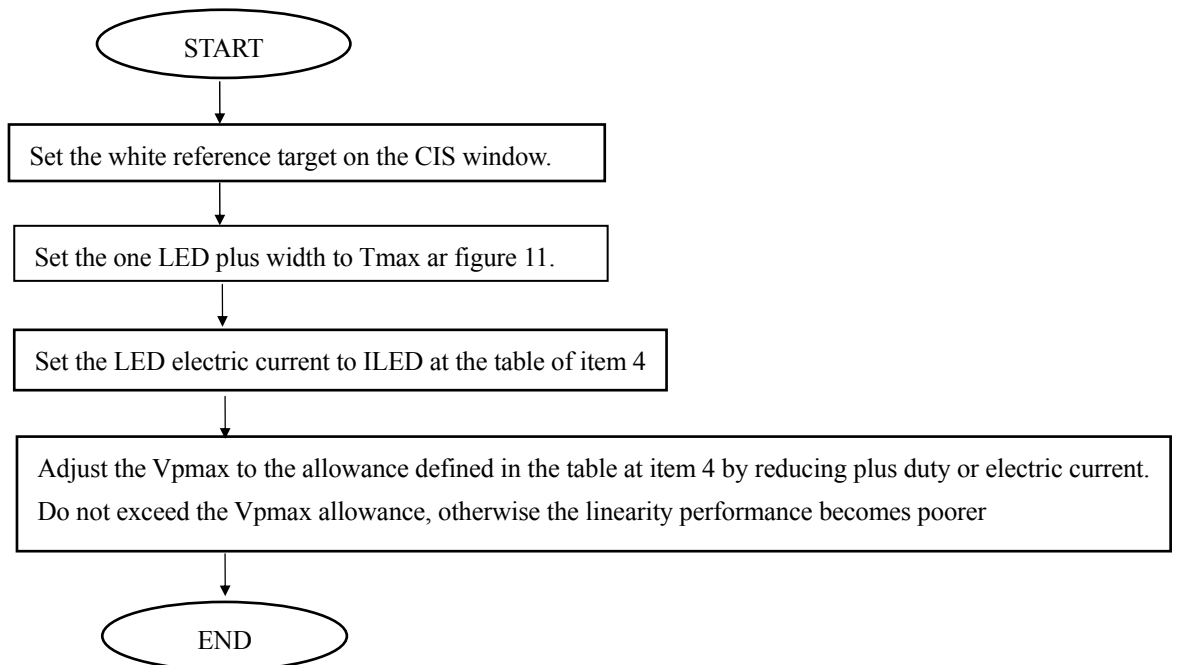
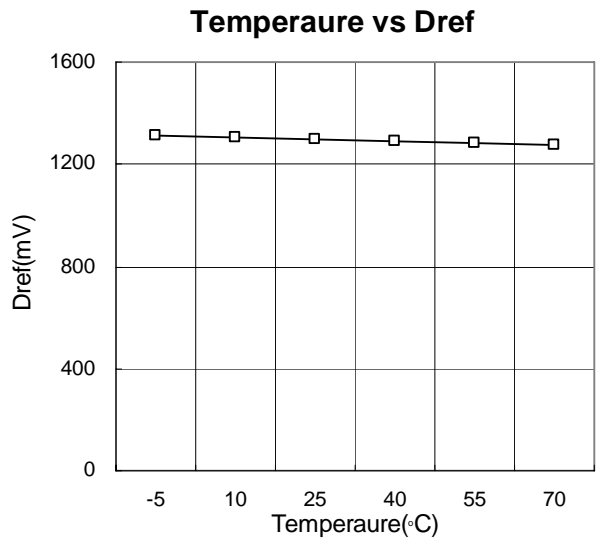
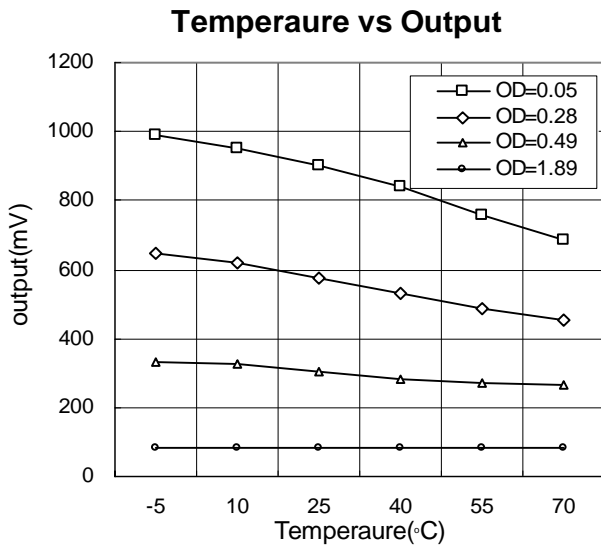
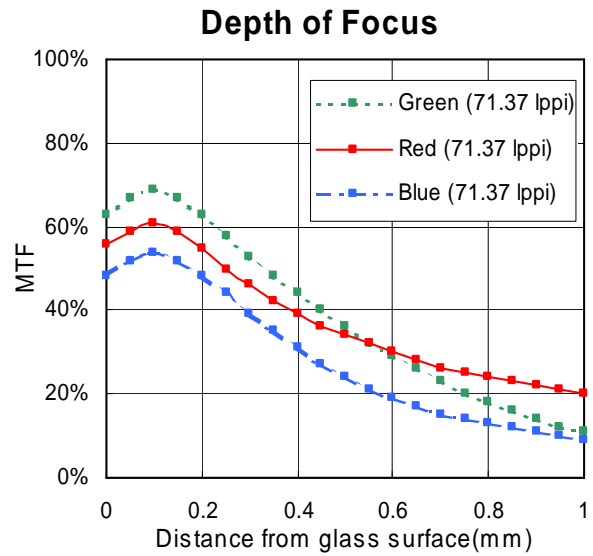
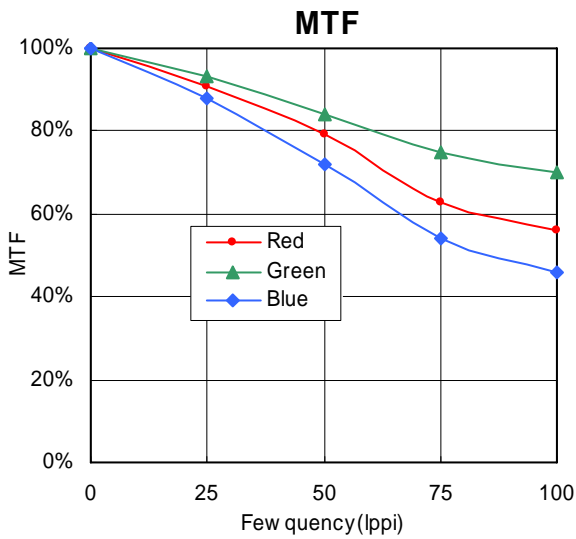
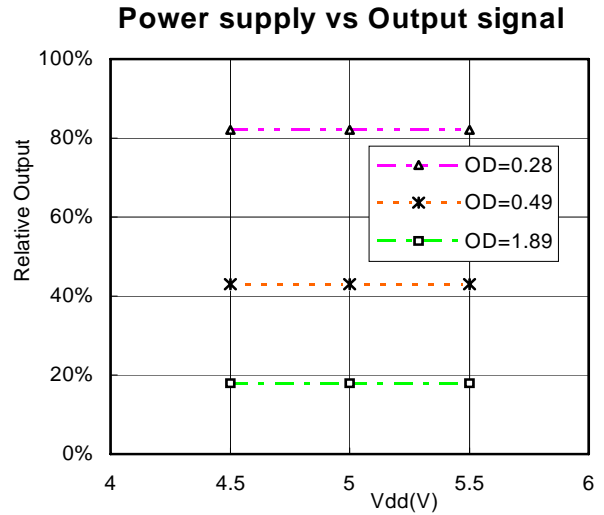
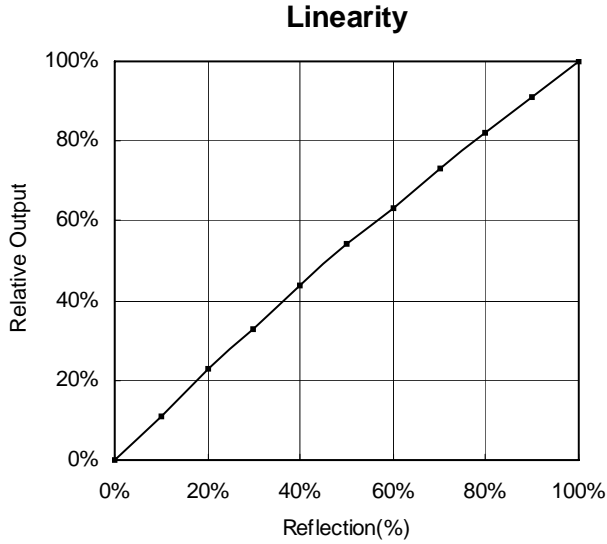
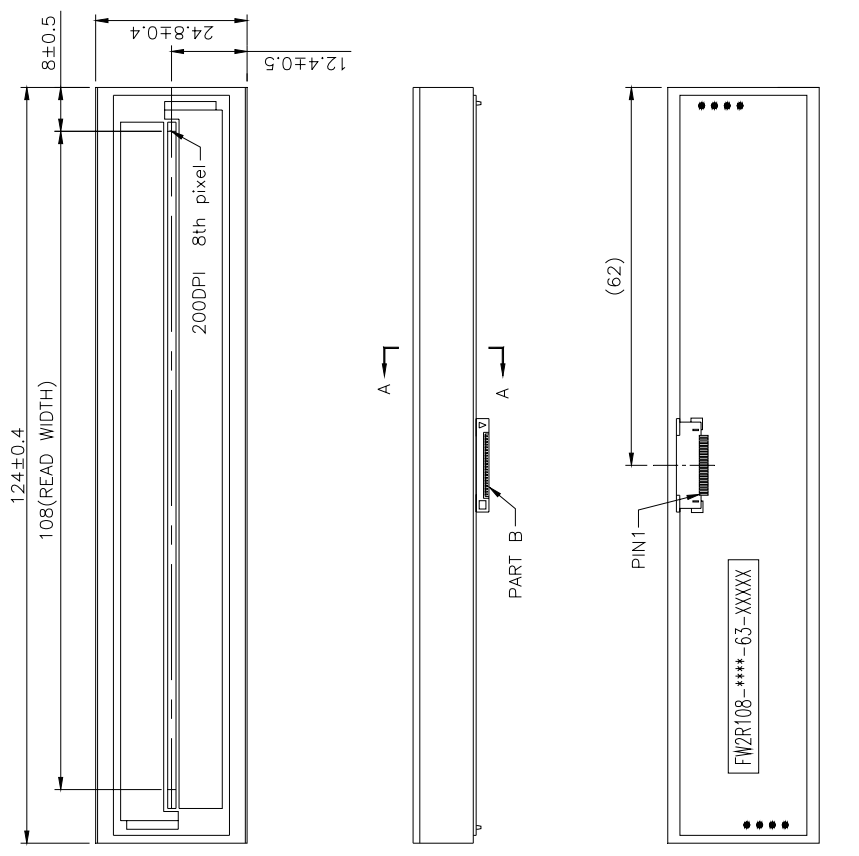
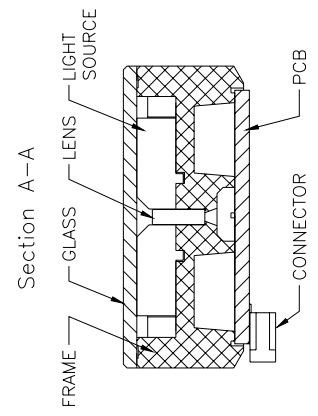
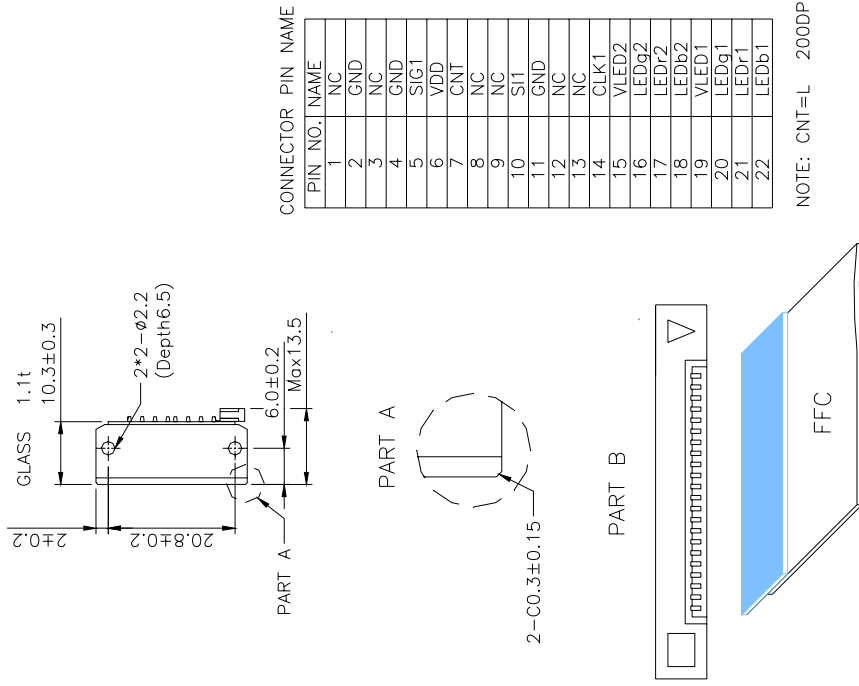


Figure 12. Flow chart of B&W mode with White Light Source Adjustment

Figure 13. Typical Performance Curve
Unless otherwise specified, Ta=25°C





- NOTE:
- CONNECTOR: 22FLZ-SM2-GB-TB(LF)(SN) OR EQUIVALENT.
 - CIS TYPE AND LOT NUMBER PASTED ON THE PCB BOTTOM.
- | | | | | |
|-------------------------------------|-------|----|----|----|
| FW2R108-****- 6 3 - XXXXX | Month | 10 | 11 | 12 |
| (CIS TYPE) (2006)(MAR) (SERIES No.) | | A | B | D |
- WHEN ATTACHING THE HOLDERS TO THE CIS, USE M2.5(M2.6) TAPPING SCREWS.
 - GLASS SHOULD NOT PROTRUDE FROM BOTH SIDE EDGE OF FRAME.